GL711FW

ATA/ATAPI to 1394
Native Bridge
Two in One Solution

SPECIFICATION 1.3
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1. Overview

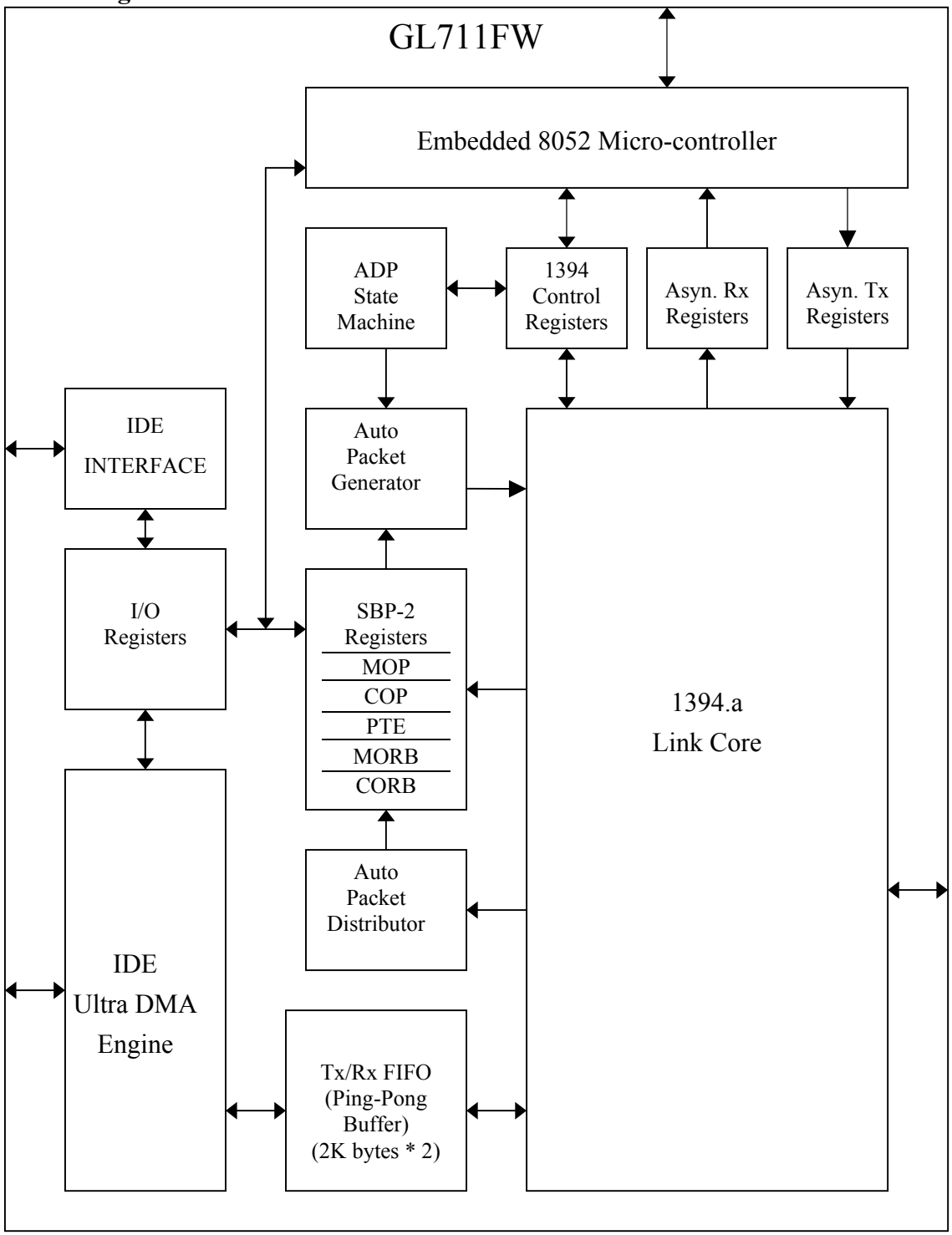
The GL711FW is a high-performance 1394 to ATA/ATAPI native bridge with an embedded SBP-2 target solution. It supports a solution for link/transaction layer controller conforming to the IEEE Std 1394 (IEEE 1394-1995 and IEEE 1394.a) up to 400Mbps transfer rate. Through the SBP-2 port driver, supported by Microsoft Windows 2000 and Windows 98 SE, Windows ME, SCSI class drivers can use SBP-2 to communicate with IEEE 1394 device using the SCSI command set. By means of the embedded 8052 processor running the firmware located in ROM (internal or optionally external) GL711FW provides an SBP-2 protocol engine to automatically achieve the transport of SCSI command and data over IEEE Std 1394 serial bus. GL711FW provides a memory interface for reading/writing firmware from/to external Flash ROM, so that it makes software download easily and helps testing, development, or other specific application purpose. GL711FW also supports an 8051 interface, which allows external 8051 to access the internal memory when the embedded 8052 was disabled for debugging and testing. The GL711FW is ideally suited to hard disk drives (HDDs), MO, CD-ROM, CD-R, CD-RW and DVD. It allows IDE drives being able to connect to a 1394 serial bus in a plug-and-play fashion. The ATA/ATAPI interface of GL711FW supports signal timing up to Ultra-DMA mode 5.

2. Features

- Data transfer rates of S100, S200 and S400
- Fully interoperable with implementation of IEEE-1394(1995) and IEEE 1394.a-2000 compliant
- Standard PHY/link Interface
- Firmware support for SBP-2 target agent
- Fully ATA/ATAPI-6 compliant.
- Supports IDE PIO modes and DMA modes and Ultra DMA modes up to UDMA100.
- Embedded RAM, ROM and micro-processor.
- External Flash ROM interface for easy updating firmware code.
- Automatic SBP-2 protocol management by an internal hardware engine to improve performance and firmware efficiency
- Auto acknowledge-code response for all packets that targeted to Management/Command ORB agent SBP-2 protocol engine:
  - Automatic Management ORB fetch
  - Linked Command ORB fetch
  - Auto address increment DMA for both direct and indirect addressing
- Automatic Page Table fetching
- Dedicated asynchronous data transfer
- Automatic packing/de-packing for asynchronous transmit/receive data of DMA
- Automatic single-retry protocol and split transaction control.
- 2 sets of 4-quadlet registers for Asynchronous Receive/Transmit packet header
- 2 sets of 8-quadlet registers for general Asynchronous Receive/Transmit packet data block payload
- 5 sets of 8/8/2/2/2-quadlet registers for Receive packet data block payload dedicated for SBP-2 requirement (MORB,
- CORB, PTE, MOP and COP)
- 4K bytes of FIFO for bi-directional transmit/receive data

3. Function Block

Block Diagram



Functional Overview

The GL711FW is designed to simplify the firmware issue of μP (8052) and save hardware cost. Upon the completion of a packet reception, the GL711FW will automatically respond acknowledge code according to the destination offset and generate the corresponding interrupt to inform the firmware to check if the received packet meets SBP-2 and 1394 protocol or not. The data payload dedicated to SBP-2 protocol is moved to the specified registers so that firmware can easily inquire and reply the data packet according to the received packet if necessary. The μP has to do is to set "1394 instruction register" properly and then the internal SBP-2 engine will automatically collect all fields from SBP-2 registers to generate the data packet. For the SCSI command that requested from initiator, firmware have to transfer these commands to ATA/ATAPI commands, and write them to IDE device through I/O register to access IDE interface. The embedded μP and internal ROM can be disabled by negating ENUP# and EA respectively for prototype development or other specific functions.

GL711FW architecture:

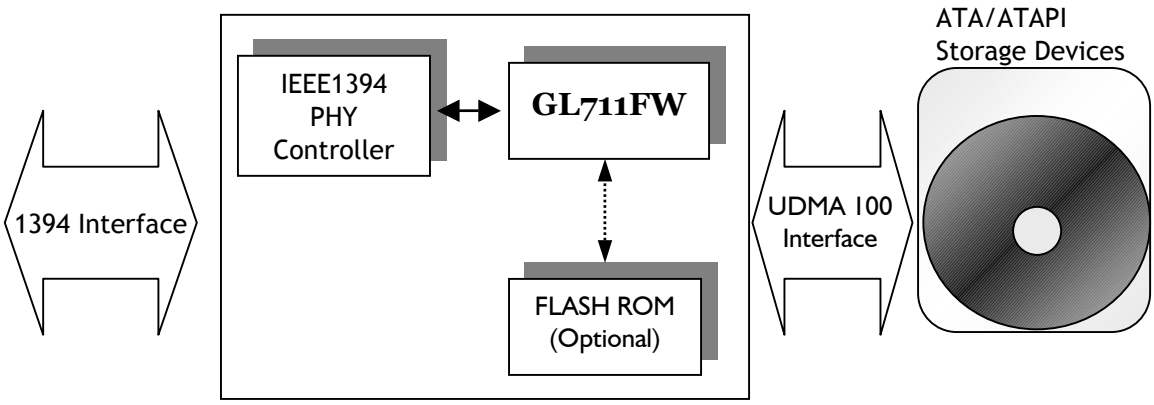
1. **Asyn Tx registers:** general asynchronous packet transmit registers, 4-quadlets for 1394 header and 8-quadlets for data payload. After getting all fields of packet ready, the firmware can set “AsynTx” instruction to send the packet. Some packets for transmitting packets like “Login Response”, “Query Login Response” and “Status Block” are prepared by the registers whose maximum data payload is 8 quadlets.
2. **Asyn Rx registers:** general asynchronous packet receives registers, 4-quadlets for 1394 header and 8-quadlets for data payload. The received packet other than the SBP-2 associated read response packets, like "Config ROM Read Request" from the initiators, is stored in the registers. However, all the SBP-2 read response packet received from the initiators are always expected by the target and forwarded to the Auto Packet Distributor.
3. **1394 Control Registers:** control and interrupt registers for IEEE 1394 and SBP-2 protocol, see the details in the section of 1394 control register.
4. **ADP State Machine:** Automatic data pipe control for SBP-2 data transfer and page table fetch.
5. **Auto Packet Generator:** generate the read or write request packet header of those packets with standard format like Config ROM read response packet, Management ORB read request, Command ORB read request, Page Table read request, Block data read request from or write request to initiator.
6. **Auto Packet Distributor:** The data payload of SBP-2 associated packet is stored at the specified registers according to its destination offset, Tlabel or last request packet command. The received data payload is classified by the GL711FW to 7 types:

Management ORB agent pointer (2 quadlets), Command ORB agent pointer (2 quadlets), Management ORB (8 quadlets), Command ORB (8 quadlets), Page Table pointer (2 quadlets), general Rx data payload (8 quadlets), and general data moved from or to initiator (1K quadlets).

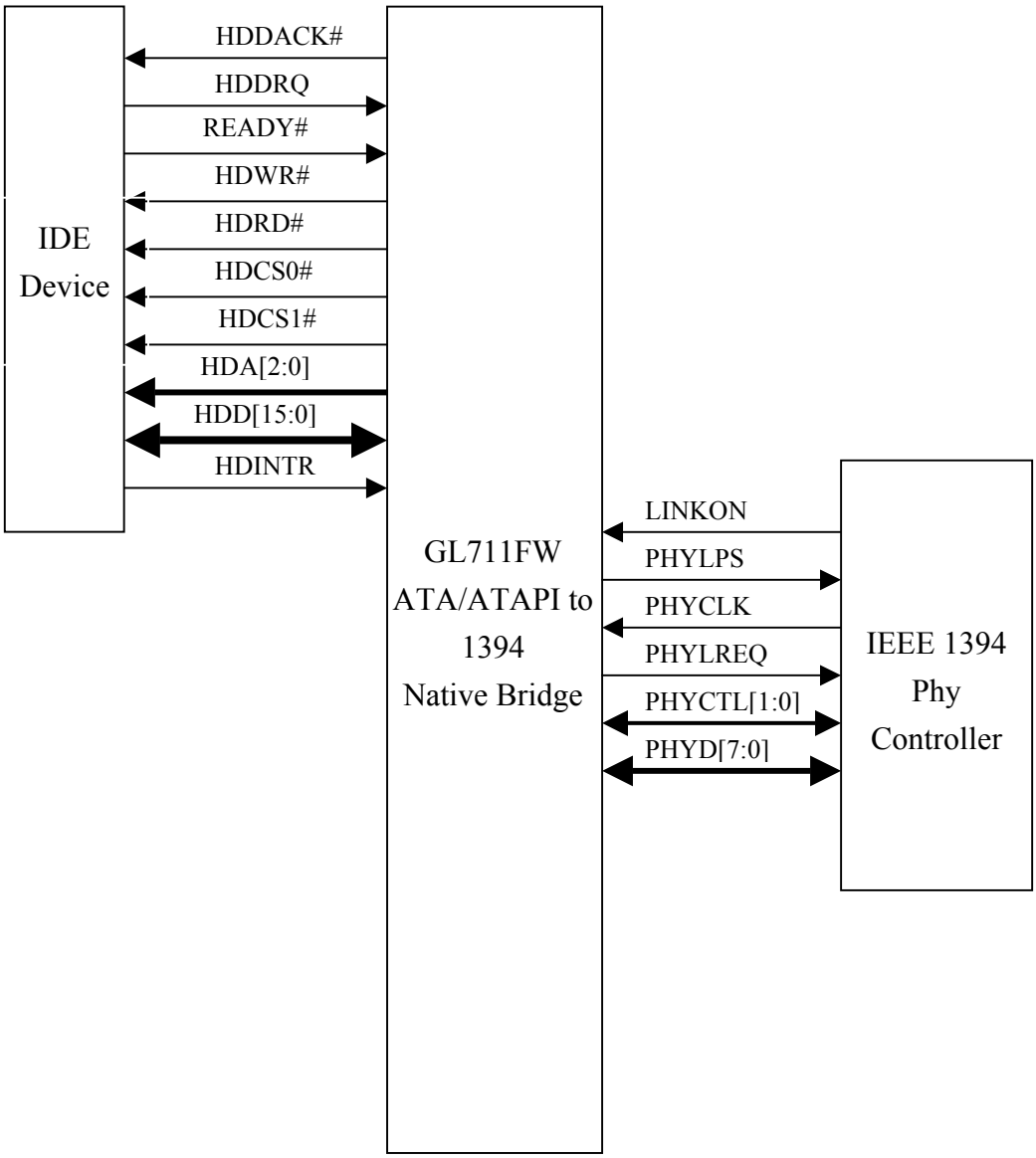
7. **SBP-2 Registers:** the registers for received data payload of SBP-2 associated packet including Management ORB agent pointer (2 quadlets), Command ORB agent pointer (2 quadlets), Management ORB (8 quadlets), Command ORB (8 quadlets) and Page Table pointer (2 quadlets).
8. **Tx/Rx Data FIFO:** 4 Kbytes of ping-pong buffer for data moved between the initiator and target.
9. **IDE Ultra DMA Engine:** control the interface to IDE device and automatically access data with IDE DMA or IDE UDMA mode.
10. **I/O Control Registers:** a register space to store information about status, packet and chip, accessible by system ASIC and μP.
11. **IDE Interface**: an interface for accessing IDE device internal registers.
12. **8051 Micro-controller**: an embedded processor for SBP2-2 to ATA/ATAPI command transaction.

4. System Configuration

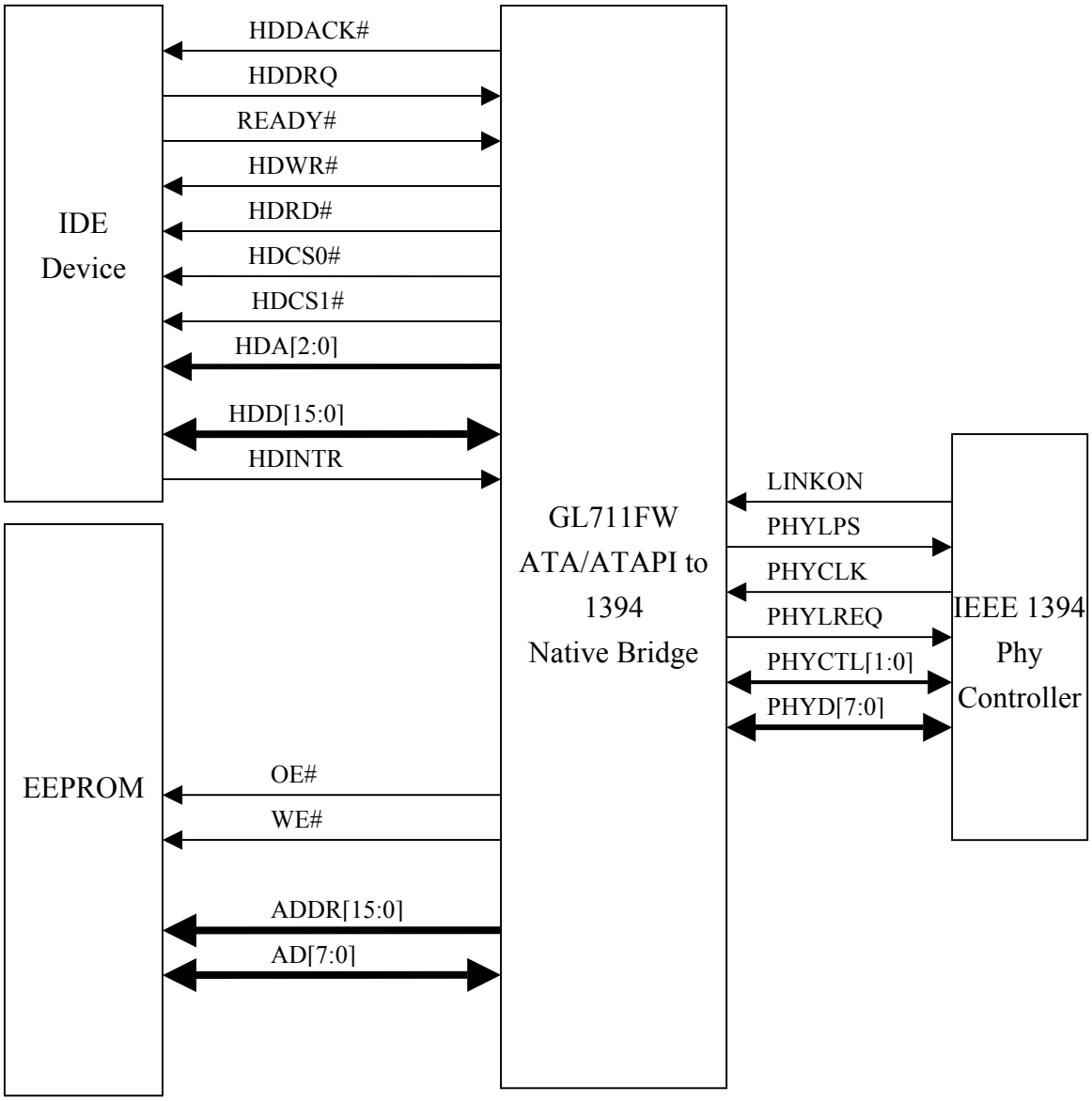
System Diagram



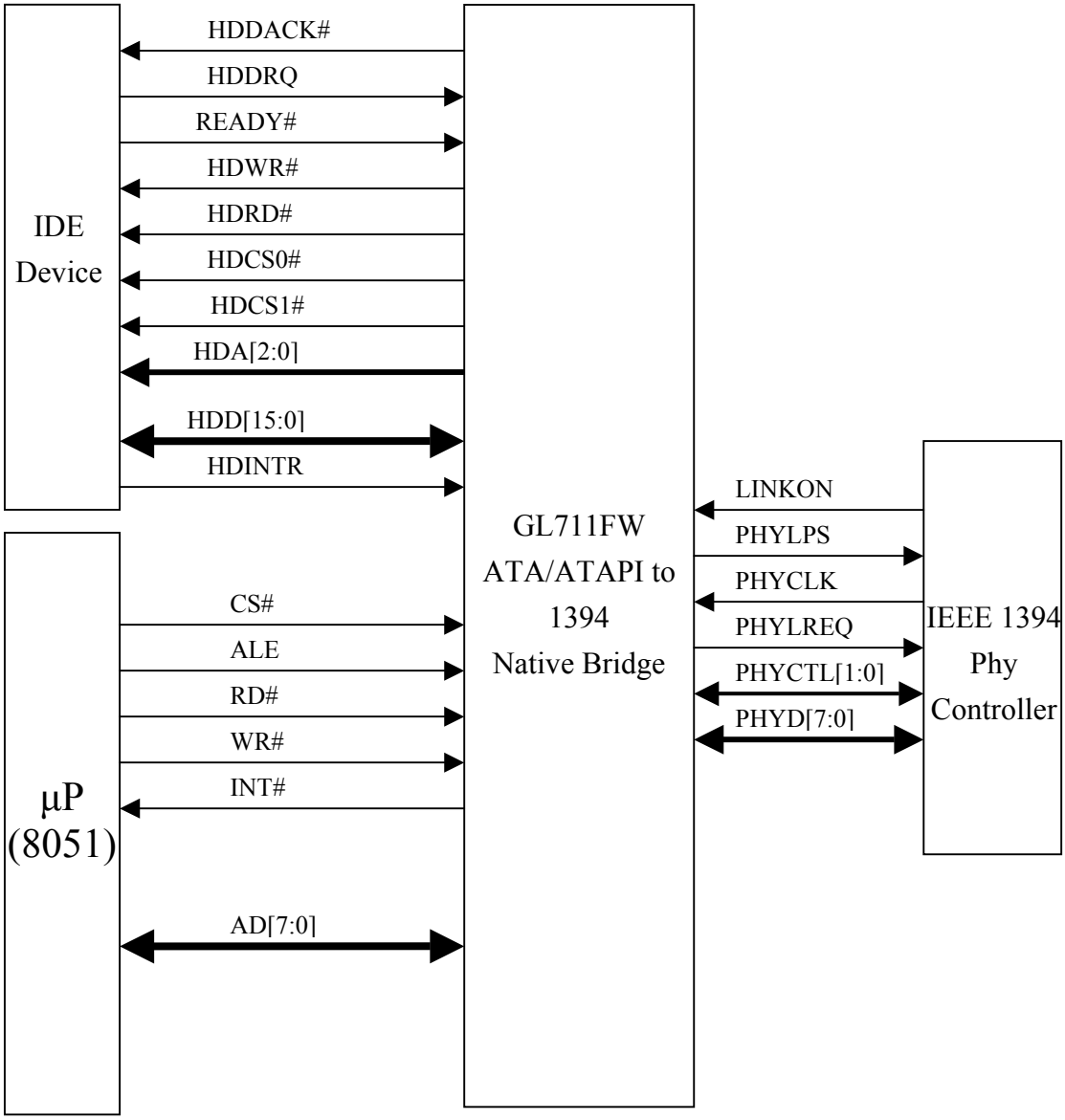
Embedded 8052 enabled and run the internal ROM code.



Embedded 8052 enabled and load the external EEPROM code.

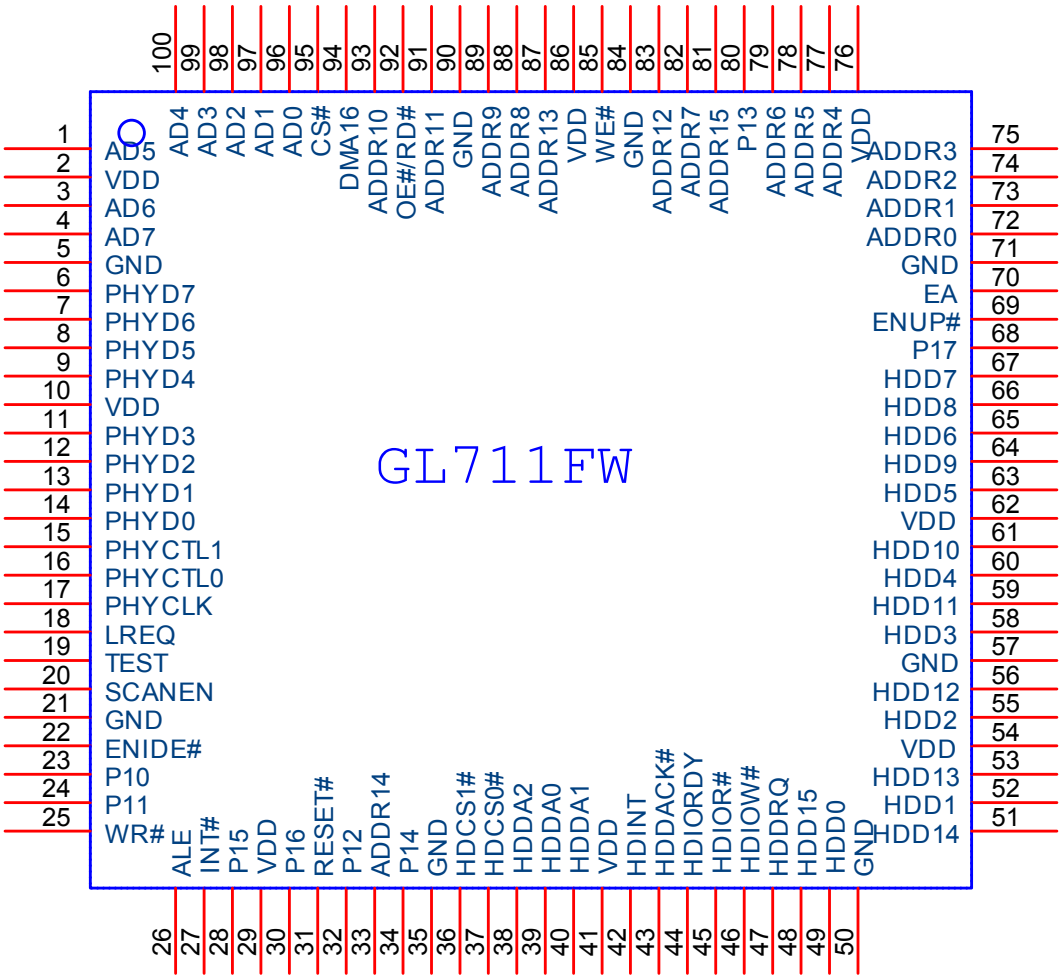


Disable embedded 8052.



5. Pin Configuration

Pin Assignment



Pin Description

PIN	SYMBOL	I/O	DESCRIPTION
Power			
31	RESET#	I	Master reset signal, low active
2,10,29, 41,54,62, 76,86	VCC	-	3.3V power supply
5,21,35, 50,57,71, 84,90	GND	-	Ground
Signals for Micro-Processor			
92	OE#/RD#	I/O	When ENUP# = '1': this active low signal enables the reading of internal register. When ENUP# = '0': this bit is used for output enable flash memory output
25	WR#	I	UP: this active low signal enables the writing of internal register.
1,3,4, 96-100	AD0-AD7	I/O	When ENUP# = '1': address & data bus bit 0 to bit 7 of external μP. When ENUP# = '0': data in-out of flash memory.
26	ALE	I	ALE is used to enable the address latch that separates the address from the data
95	CS#	I/O	When ENUP# = '1': This active low signal acts as the chip select during register access cycle. When ENUP# = '0': This bit is an active low to select flash memory.
27	INT#	O	This is an output pin to drive the active low interrupt signal to external controller.
Signals for IDE interface			
38-40	HDA0-2	O	IDE device address. The 3-bit binary coded address asserted by the ATA host to access a register or data port in the device.
37	HDCS0#	O	IDE chip select 0. The chip select signal from the ATA host used to select the Command Block registers.
36	HDCS1#	O	IDE chip select 0. The chip select signal from the ATA host used to select the Control Block registers.
46	HDIOW#(STOP)	O	Device I/O write (for PIO and Multi-word DMA mode) Stop Ultra DMA burst (for UDMA mode)

45	HDIOR#(HDMARDY#/, HDSTROBE)	O	Device I/O read (for PIO and Multi-word DMA mode) Ultra DMA host ready (for UDMA read) Ultra DMA host data strobe (for UDMA write)
48,51,53, 56,59,61, 64,66,67, 65,63,60, 58,55,52, 49	HDD15-0	I/O	IDE device data. The 8- or 16-bit data bus to/from the ATA device. Only the lower 8 bits are used for 8-bit register transfers.
44	HDIORDY(DDMARDY#/, DSTROBE)	I	I/O channel ready (for PIO and Multi-word DMA mode) Ultra DMA device ready (for UDMA write) Ultra DMA device data strobe (for UDMA read)
42	HDINT	I	IDE device interrupt: This input signal is used to interrupt the host system when interrupt pending is set.
43	HDDACK#	O	IDE DMA acknowledge: This signal is used by the ATA host to response DMARQ for DMA transfers.
47	HDDRQ	I	IDE DMA request: This signal is asserted by the ATA device when it is ready to perform a DMA data transfer to or from the ATA host when a DMA operation has been enabled.
Signals for PHY-interface			
15,16	PHY_CTL1 PHY_CTL0	I/O	Control 1 and Control 0 of the phy-link control bus. CTL1 and CTL0 indicate the four operations that can occur in this interface.
18	LREQ	O	Link request. LREQ is a output that makes bus requests and accesses the phy layer.
6-9,11-14	PHY_D7-0	I/O	Phy data7 through data0 of the phy-link data bus. Data is expected on D0-D1 for 100Mb/s packets, D0-D3 for 200Mb/s, and D0-D7 for 400Mb/s.
17	PHY_SCLK	I	System clock. PHY_SCLK is a 49.152-MHz clock from the phy.
Signals for flash memory			
81,33,87, 83,91,93, 89,88,82, 79,78,77, 75,74,73, 72	ADDR[15:0]	O	Flash PROM/EPROM address bus. ADDR15 is the most significant bit.

85	WE#	O	Flash PROM/EPROM write enable(active low). During normal operation this bit is asserting high.
Miscellaneous signals			
68,30,28, 34,80,32, 24,23	P17-P10	I/O	GPIO for firmware use
94	DMA16	I	This bit is used to enable 16-bits DMA function.
19	TEST	I	This bit is used only in test mode. This bit must tie low in normal .
20	SCANEN	I	This bit is used only in test mode. This bit must tie low in normal .
22	ENIDE#	I	For enable IDE function, active low.
69	ENUP#	I	For enable internal 8052 function, active low.
70	EA	I	For enable external ROM.

6. Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage Range, (VCC)	-0.3V to 3.6V
Input Voltage Range	-0.3V to (VCC+0.3V)
Output Voltage Range	-0.3V to (VCC+0.3V)
Operating temperature	0°C to 70°C
ESD Human Body Model	7 kV

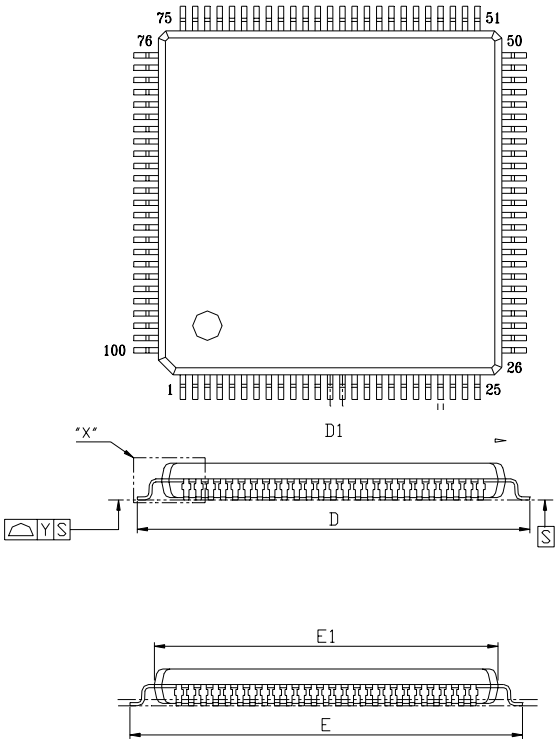
Recommended Operation Conditions

	NOM.	MIN.	MAX.	UIITS
Supply voltage	3.3	3.0	3.6	V
Input voltage		0	VCC	V
Output voltage			VCC	V
High-level input voltage, VIH		0.7VCC	VCC	V
Low-level input voltage, VIL		0	0.3VCC	V
Operating Temperature	25	0	70	0°C

Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UIITS
High-level output voltage, Voh	Ioh = -12mA Ioh= -8mA	0.8VCC		V
Low-level output voltage, Vol	Iol = 12mA Iol= 8mA		0.2VCC	V

7. Package Dimension



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	9
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		